9. (Amended) The silicon on insulator transistor structure of claim 8, further including a backgate adjacent the channel region, and on an opposing side of the channel region from the gate, and forming a junction with the channel region, the backgate comprising the first semiconductor material and a second semiconductor with an energy gap greater than the device layer semiconductor and being doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

A4

10. (Amended) The silicon on insulator transistor structure of claim 9, wherein the first semiconductor material is silicon.

Attached hereto is an appendix that includes the above amendments in annotated form.

REMARKS

Claims 1-14 are presently under consideration. Claims 1, 3, and 8-10 have been amended herein. New claims 22-27 have been added. Favorable reconsideration of the application, as amended, is respectfully requested.

I. CLAIM OBJECTIONS

The examiner has objected to claim 3 and recommended that the term "fist" be changed to "first". The applicant has corrected the misspelling.

II. REJECTION OF CLAIMS UNDER 35 USC § 102

Claims 1-4 and 8-11 stand rejected under 35 USC 102(e) as being anticipated by US patent 6,248,626 to Kumar et al. The Examiner asserts that Kumar et al. teaches a device that includes all of the elements of claim 1.

Both independent claims 1 and 8 define a transistor structure that comprises a central channel region consisting of a first semiconductor lightly doped with a first impurity element to increase first conductivity free carriers. A source region and a drain region are positioned on opposing sides of the central channel region and both the

source region and the drain region consist of the first semiconductor heavily doped with the first impurity element. A gate is positioned adjacent to the channel region and forms a junction with the channel region. The gate comprises the first semiconductor and a second semiconductor with an energy gap greater than the first semiconductor. The gate is also doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

Claims 2 and 9 define the transistor structure of claims 1 and 8 respectively which further includes a backgate adjacent to the channel region, forming a junction with the channel region, and on an opposing side of the channel region. The backgate also comprises the first semiconductor and a second semiconductor with an energy gap greater than the first semiconductor and is also doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

Claims 3 and 10 define the transistor structure of claims 2 and 9 respectively whereby the first semiconductor is silicon. Claims 4 and 11 define the transistor structure of claims 3 and 10 respectively whereby the second semiconductor s carbon.

Applicants, respectfully submit that Kumar et al. does not teach that upon which the Examiner relies in making the rejection. Kumar et al. teaches an EEPROM memory cell with a floating back gate for charge storage. In an alternative, as shown in Figure 2a, the back gate may be coupled to circuitry (as opposed to floating) to control the threshold voltage and to the carriers at the gates oxide/silicon interface. Both embodiments of the Kumar et al. device include a traditional field effect transistor structure that includes an oxide film between the channel region and both the gate and the back gate. As such, neither the gate nor the back gate of Kumar et al. forms a junction with the channel region.

US Patent 5,753,938 to Thapar et al. and US Patent 4,484,207 to Nishizawa et al. (both submitted in an information disclosure attached hereto) disclose an array of vertical static induction transistors that includes a drain layer positioned below a channel (or drift) layer. Gate wells protrude downward into the drift layer and remain isolated from the drain layer by a portion of the drift layer thereby forming channel mesas within the drift layer between the gate wells. Source regions are positioned at

the top of the channel mesas, between the gate wells, and are isolated from the gate wells by either an oxide or a portion of the channel mesa.

The drift region may be lightly doped n- while the source regions and the drain regions are heavily doped n-. The gate wells are doped p+. Nishizawa et al. teaches that the source region may comprise a semiconductor material having a great band gap such that the region between the source and the gate regions will present a hetero-junction with the intervention of the channel region. Thapar et al. teaches that the entire substrate in which the drain layer, channel layer, gate wells, and source regions are formed may be mono-crystalline silicon carbide.

Neither Kumar et al., Thapar et al., Nishizawa et al., nor the other art of record, alone, or in combination, discloses a transistor structure that comprises a central channel region consisting of a first semiconductor lightly doped with a first impurity element to increase first conductivity free carriers. A source region and a drain region are positioned on opposing sides of the central channel region and both the source region and the drain region consisting of the first semiconductor heavily doped with the first impurity element. A gate is positioned adjacent to the channel region and forms a junction with the channel region. The gate comprises the first semiconductor and a second semiconductor with an energy gap greater than the first semiconductor. The gate is also doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

III. REJECTION OF CLAIMS UNDER 35 USC § 103

Claims 5-7 and 12-14 stand rejected under 35 USC 103(a) based on being unpatentable over Kumar et al. in view of US Patent 6,274,887 to Yamazaki et al.

The examiner admits that Kumar fails to explicitly teach that the first conductivity free carriers are electron and the second conductivity free carriers are holes. The Examiner relies on Yamazaki teaching that doping with Arsenic forms an N-type region wherein the carriers are electrons and that doping with Boron forms a P-type region whereby the carriers are holes.

As discussed with respect to the rejection under 35 USC §102, neither Kumar et al., Thapar et al., Nishizawa et al., Yamazaki et al., nor the other art of record, alone, or in combination, discloses a transistor structure of independent claims 1 and 8. The additional limitations set forth in claims 5-7 and 12-14 (and all intervening claims) futher distinguish such claims.

IV. CONCLUSION

Accordingly, claims 1-14 and 22-27 are believed to be allowable and the application is believed to be in condition for allowance. A prompt action to such end is earnestly solicited.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should a petition for an extension of time be necessary for the timely reply to the outstanding Office Action (or if such a petition has been made and an additional extension is necessary), petition is hereby made and the Commissioner is authorized to charge any fees (including additional claim fees) to Deposit Account No. 18-0988.

Respectfully submitted,

RENNER, OTTO, BOISSELLE & SKLAR, P.L.L.

Mark D. Saralino
Reg. No. 34,243

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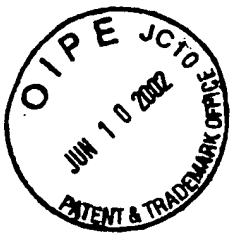

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June 3, 2002
DATE

APPENDIX

IN THE CLAIMS:

Please amend claims 1, 3 and 8-10 as follows:

1. (Amended) A transistor structure comprising:

a) a central channel region [comprising] consisting of a first semiconductor lightly doped with a first impurity element to increase first conductivity free carriers;

b) a source region and a drain region on opposing sides of the central channel region, both source region and the drain region [being] consisting of the first semiconductor heavily doped with the first impurity element;

c) a gate adjacent the channel region and forming a junction with the channel region, the gate comprising the first semiconductor and a second semiconductor with an energy gap greater than the first semiconductor and being doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

3. (Amended) The transistor structure of claim 2, wherein the [fist] first semiconductor is silicon.

8. (Amended) A silicon on insulator transistor structure comprising:

a) an insulating oxide layer separating a device layer of semiconductor material from a bulk semiconductor base region;

b) a generally rectangular central channel region within the device layer, the central channel region consisting of a first semiconductor material doped with a first impurity element to increase first conductivity free carriers;

c) a source region and a drain region on opposing sides of the generally rectangular central channel region, both the source region and the drain region consisting of the first semiconductor material [comprising the device layer semiconductor material] heavily doped with the first impurity element;

d) a gate adjacent the channel region and extending along a side of the central channel region adjacent the source region and forming a junction with the channel region, the gate comprising the [device layer semiconductor] first semiconductor material and a second semiconductor with an energy gap greater than the [device layer semiconductor] first semiconductor material and being doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

9. (Amended) The silicon on insulator transistor structure of claim 8, further including a backgate adjacent the channel region, and on an opposing side of the channel region from the gate, and forming a junction with the channel region, the backgate comprising the [device layer semiconductor] first semiconductor material and a second semiconductor with an energy gap greater than the device layer semiconductor and being doped with a second impurity element to increase carriers of the opposite conductivity as the first free carriers.

10. (Amended) The silicon on insulator transistor structure of claim 9, wherein the [fist] first semiconductor material is silicon.